


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) |

Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "(simulation <and> (multi-core <sentence> processor) <in>metadata)) <and>..."

☐ e-mail

Your search matched 4 of 1428539 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

[View Session History](#)
[New Search](#)

Modify Search

☐ Check to search only within this results set
Display Format: ☒ Citation ☐ Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

[Select All](#)
[Deselect All](#)

- ☐ 1. **Single-ISA heterogeneous multi-core architectures: the potential for proc reduction**
 Kumar, R.; Farkas, K.I.; Jouppi, N.P.; Ranganathan, P.; Tullsen, D.M.; [Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM International Symposium on](#)
 2003 Page(s):81 - 92
 Digital Object Identifier 10.1109/MICRO.2003.1253185
[AbstractPlus](#) | Full Text: [PDF](#)(420 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ 2. **Exploiting the cache capacity of a single-chip multi-core processor with migration**
 Michaud, P.; [High Performance Computer Architecture, 2004. HPCA-10. Proceedings. 10th Symposium on](#)
 14-18 Feb. 2004 Page(s):186 - 195
 Digital Object Identifier 10.1109/HPCA.2004.10026
[AbstractPlus](#) | Full Text: [PDF](#)(384 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ 3. **HiBRID-SoC: a multi-core system-on-chip architecture for multimedia signal applications**
 Stolberg, H.-J.; Berekovic, M.; Friebe, L.; Moch, S.; Flugel, S.; Xun Mao; Kulac Klusmann, H.; Pirsch, P.; [Design, Automation and Test in Europe Conference and Exhibition, 2003](#)
 2003 Page(s):8 - 13 suppl.
 Digital Object Identifier 10.1109/DATE.2003.1253797
[AbstractPlus](#) | Full Text: [PDF](#)(433 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ 4. **Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architecture**
 Kumar, R.; Farkas, K.; Jouppi, N.P.; Ranganathan, P.; Tullsen, D.M.; [Computer Architecture Letters, IEEE](#)
 Volume 2, Issue 1, Jan. 2003 Page(s):2 - 2
 Digital Object Identifier 10.1109/L-CA.2003.6
[AbstractPlus](#) | Full Text: [PDF](#)(736 KB) IEEE JNL
[Rights and Permissions](#)